Fig. 1

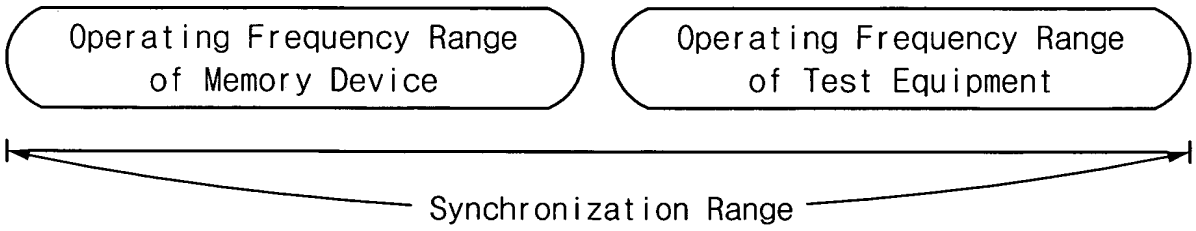

Operating Frequency Range of Memory Device
Operating Frequency Range of Test Equipment
Synchronization Range

Fig. 2

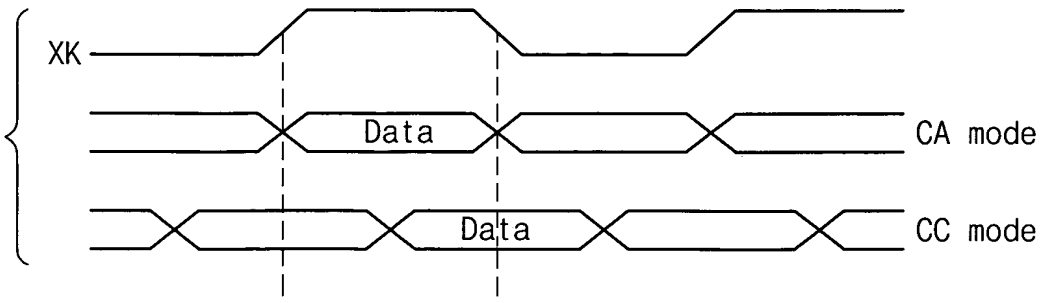

XK
Data
CA mode
Data
CC mode

Fig. 3

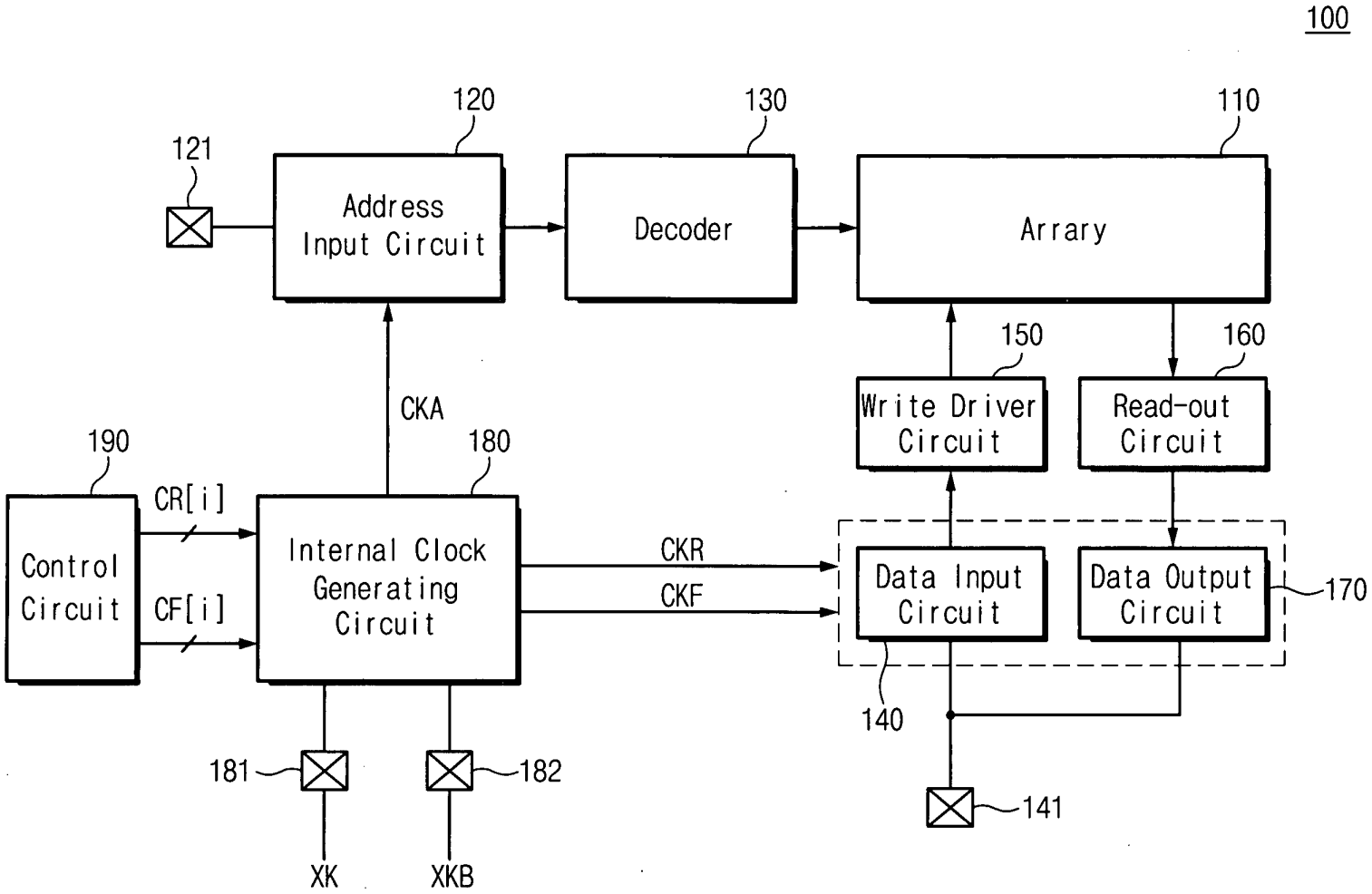

100
120
130
110
121
Address Input Circuit
Decoder
Arrary
150
160
Write Driver Circuit
Read-out Circuit
CKA
190
180
CR[i]
Control Circuit
CF[i]
Internal Clock Generating Circuit
CKR
CKF
Data Input Circuit
Data Output Circuit
170
140
181
182
141
XK
XKB

Fig. 4A

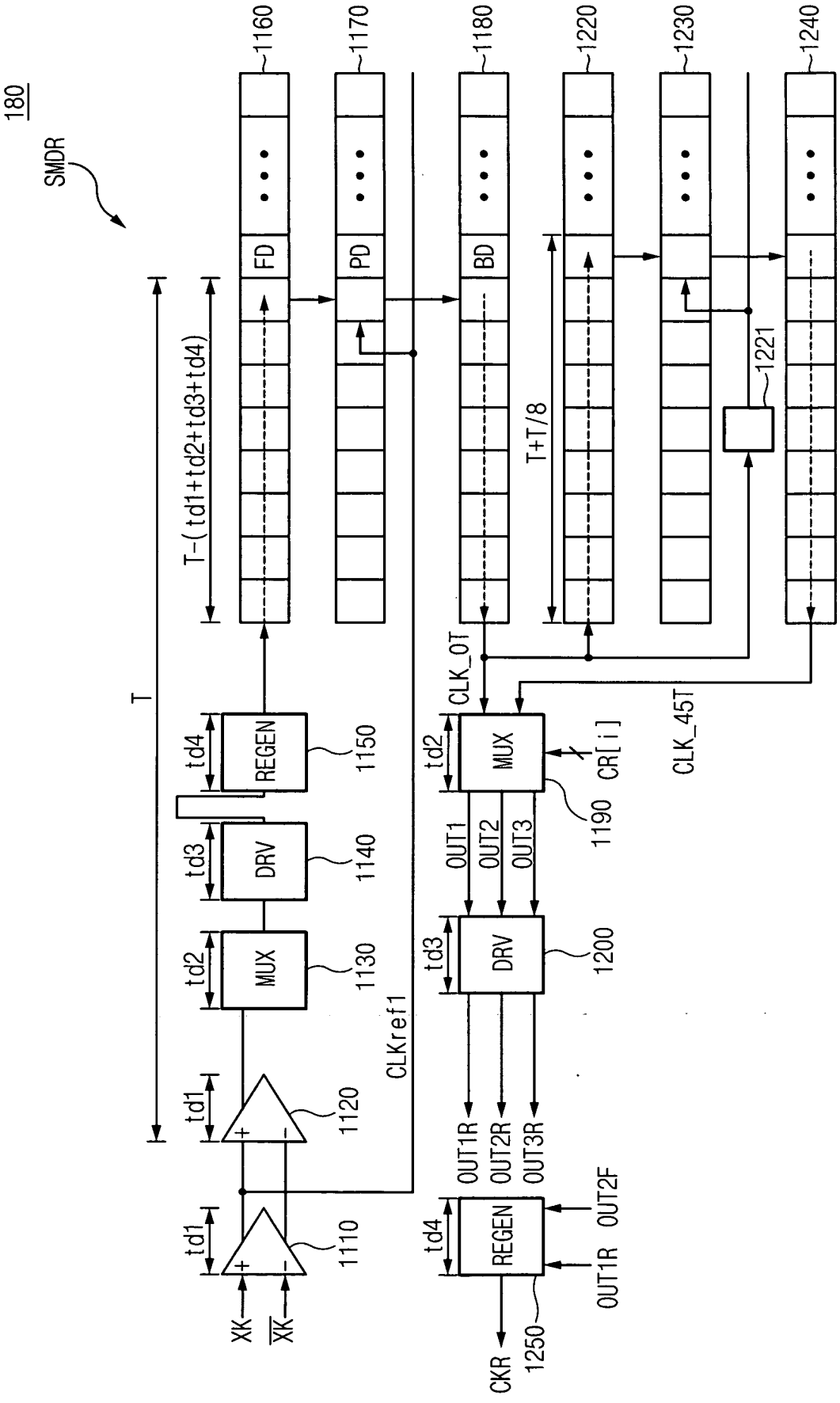

180
SMDR
T
T-(td1+td2+td3+td4)
T+T/8
td1
td2
td3
td4
XK
/XK
1110
1120
MUX
1130
DRV
1140
REGEN
1150
FD
PD
BD
1160
1170
1180
1220
1230
1240
1221
CLKref1
CLK_0T
CLK_45T
CR[i]
1190
OUT1
OUT2
OUT3
1200
OUT1R
OUT2R
OUT3R
OUT2F
CKR
1250

Fig. 4B

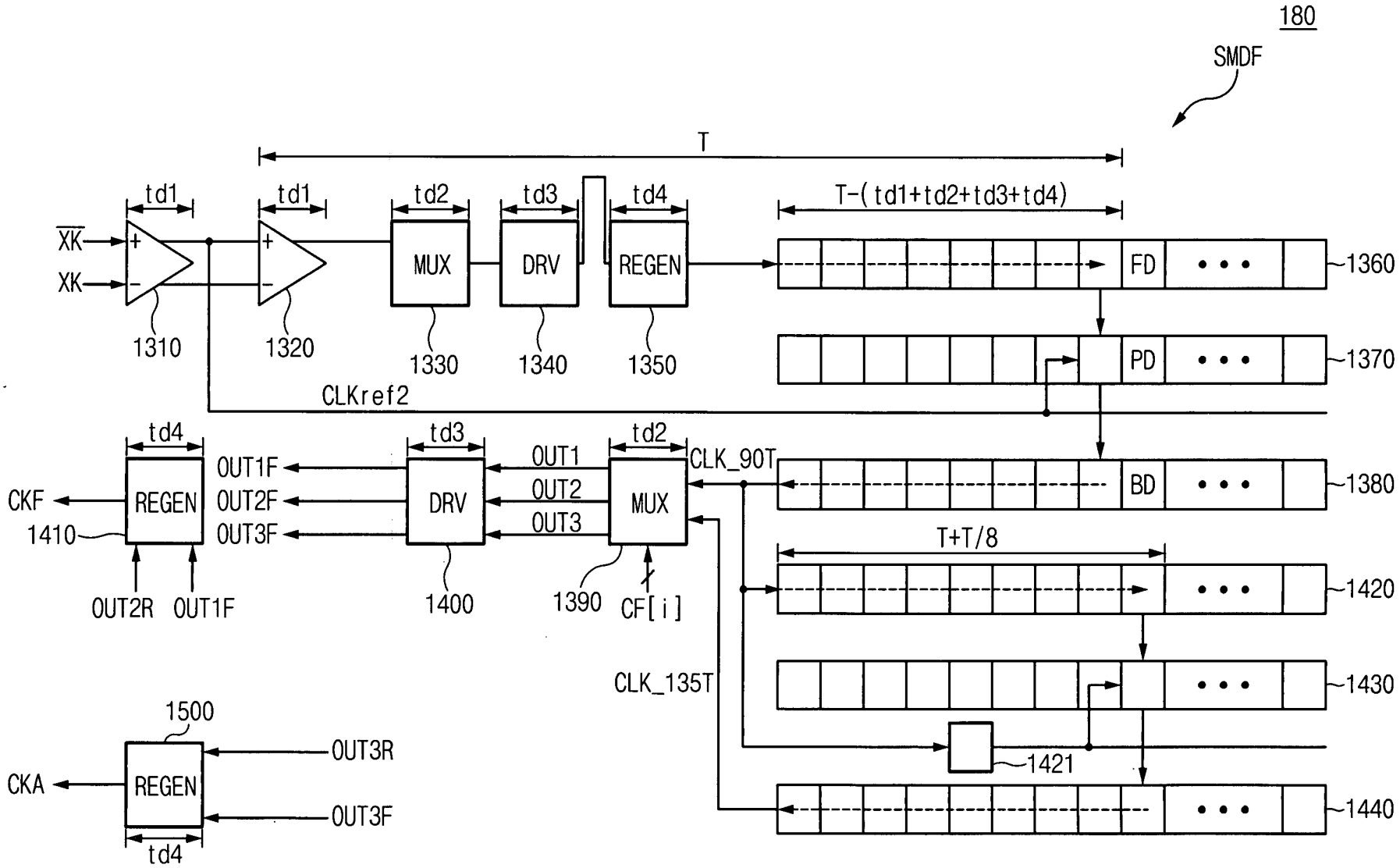

180
SMDF
T
td1
td1
td2
td3
td4
T-(td1+td2+td3+td4)
XK
XK
MUX
DRV
REGEN
FD
PD
BD
1310
1320
1330
1340
1350
1360
1370
1380
CLKref2
td4
td3
td2
OUT1
OUT2
OUT3
CLK_90T
CKF
REGEN
OUT1F
OUT2F
OUT3F
DRV
MUX
1410
OUT2R
OUT1F
1400
1390
CF[i]
T+T/8
1420
1430
CLK_135T
1421
1440
1500
CKA
REGEN
OUT3R
OUT3F
td4

Fig. 5

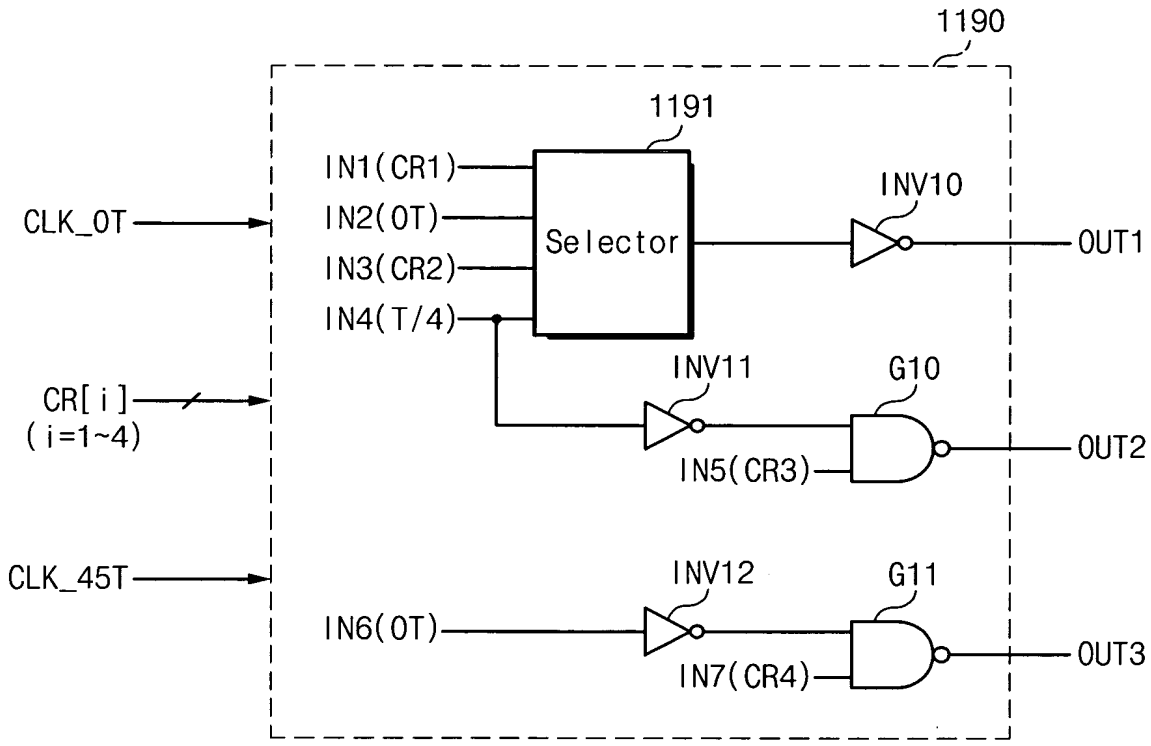

1190
1191
IN1(CR1)
IN2(0T)
IN3(CR2)
IN4(T/4)
Selector
INV10
OUT1
CLK_0T
CR[i]
(i=1~4)
INV11
G10
IN5(CR3)
OUT2
CLK_45T
INV12
G11
IN6(0T)
IN7(CR4)
OUT3

Fig. 6

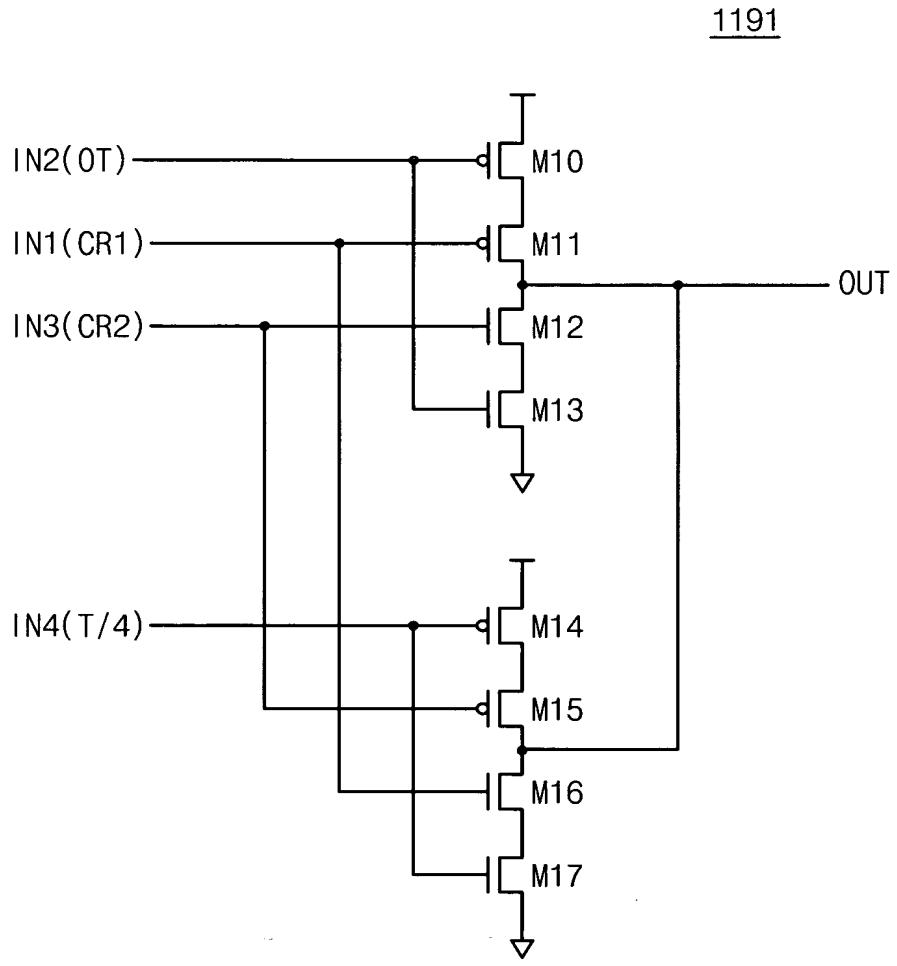

1191
IN2(OT)
IN1(CR1)
IN3(CR2)
IN4(T/4)
M10
M11
M12
M13
M14
M15
M16
M17
OUT

Fig. 7A

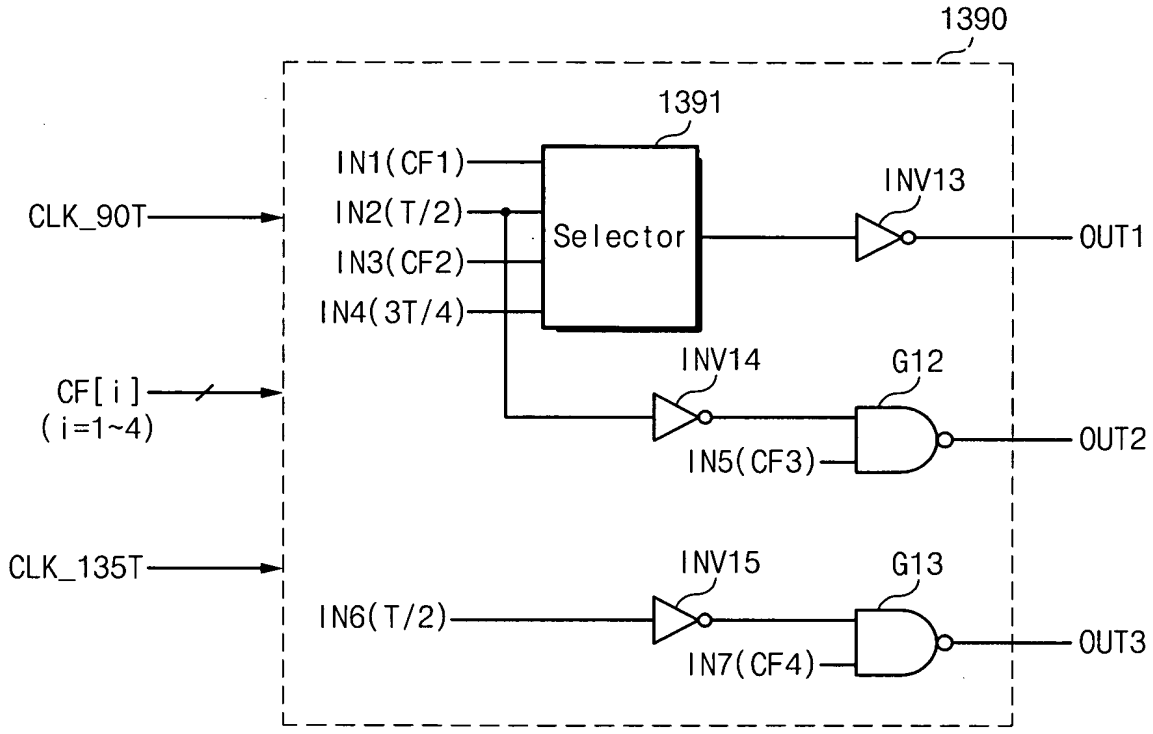

1390
1391
IN1(CF1)
IN2(T/2)
IN3(CF2)
IN4(3T/4)
Selector
INV13
OUT1
CLK_90T
CF[i]
(i=1~4)
INV14
G12
IN5(CF3)
OUT2
CLK_135T
INV15
G13
IN6(T/2)
IN7(CF4)
OUT3

Fig. 7B

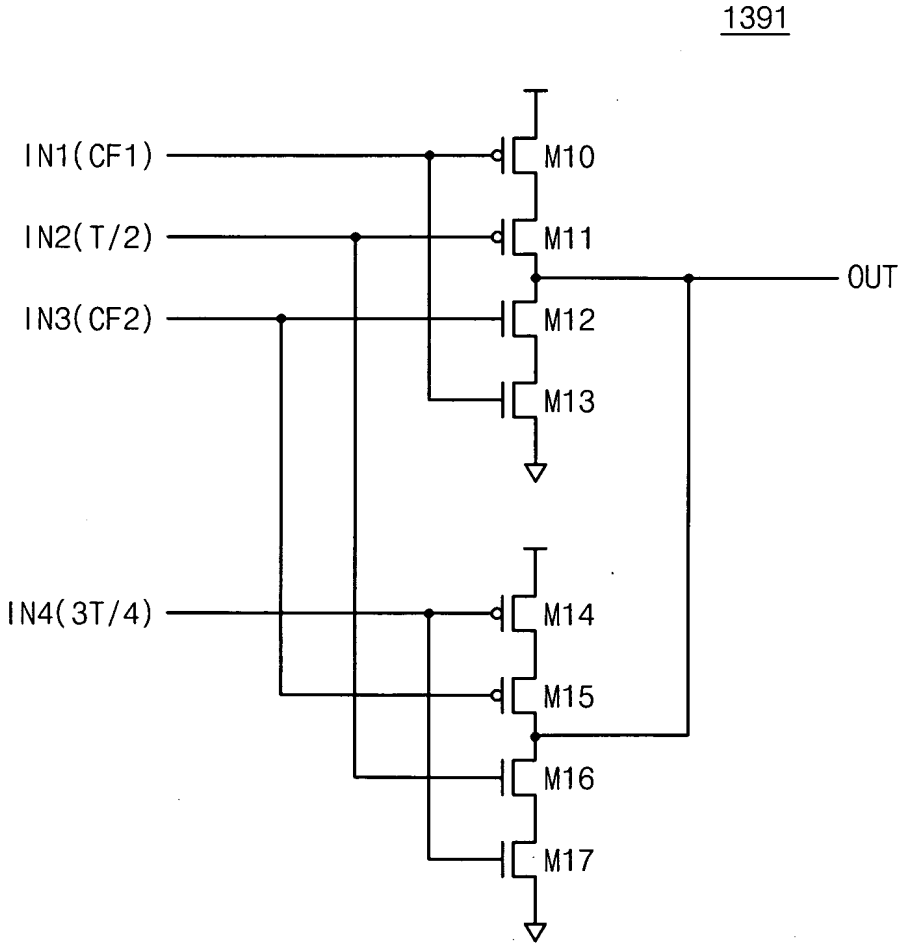

1391
IN1(CF1)
IN2(T/2)
IN3(CF2)
IN4(3T/4)
M10
M11
M12
M13
M14
M15
M16
M17
OUT

Fig. 8

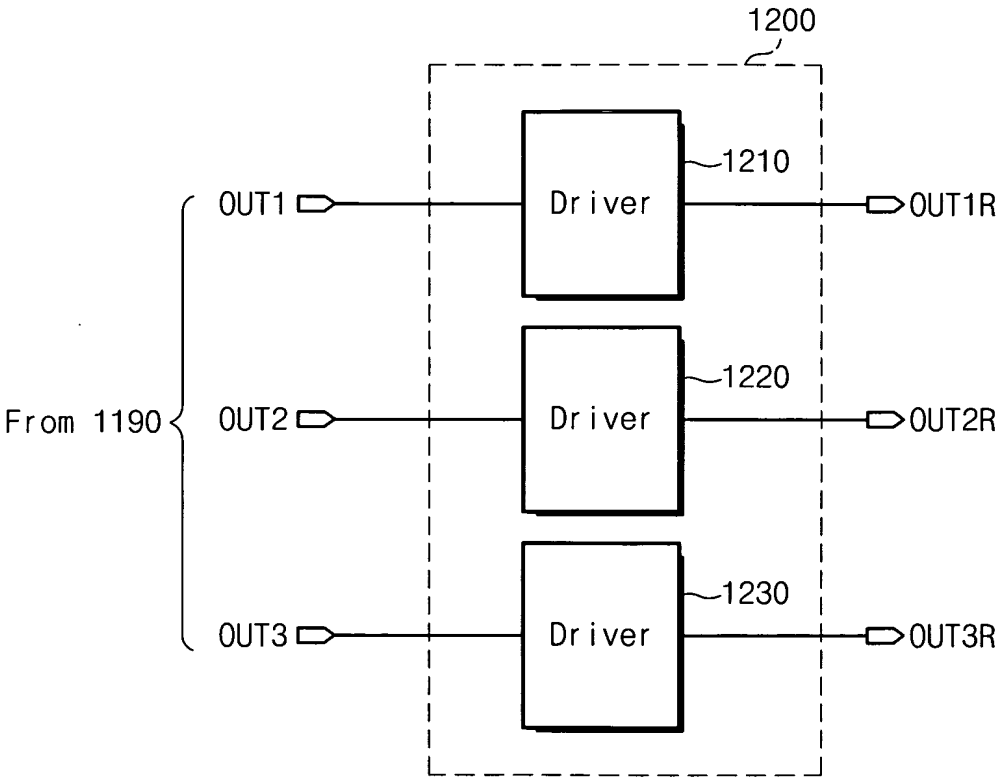

1200
1210
Driver
OUT1
OUT1R
1220
Driver
From 1190
OUT2
OUT2R
1230
Driver
OUT3
OUT3R

Fig. 9

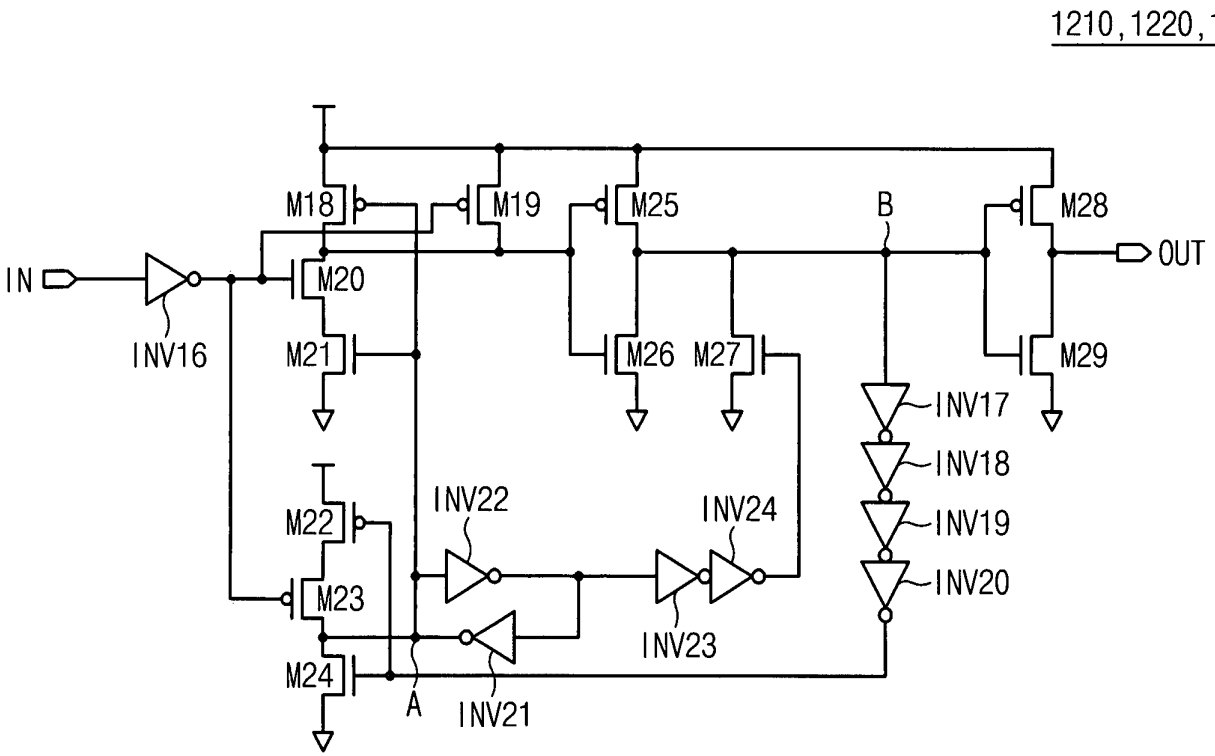

1210,1220,1230
M18
M19
M25
B
M28
IN
M20
OUT
INV16
M21
M26
M27
M29
INV17
INV18
INV19
INV20
M22
INV22
INV24
M23
INV23
M24
A
INV21

Fig. 10

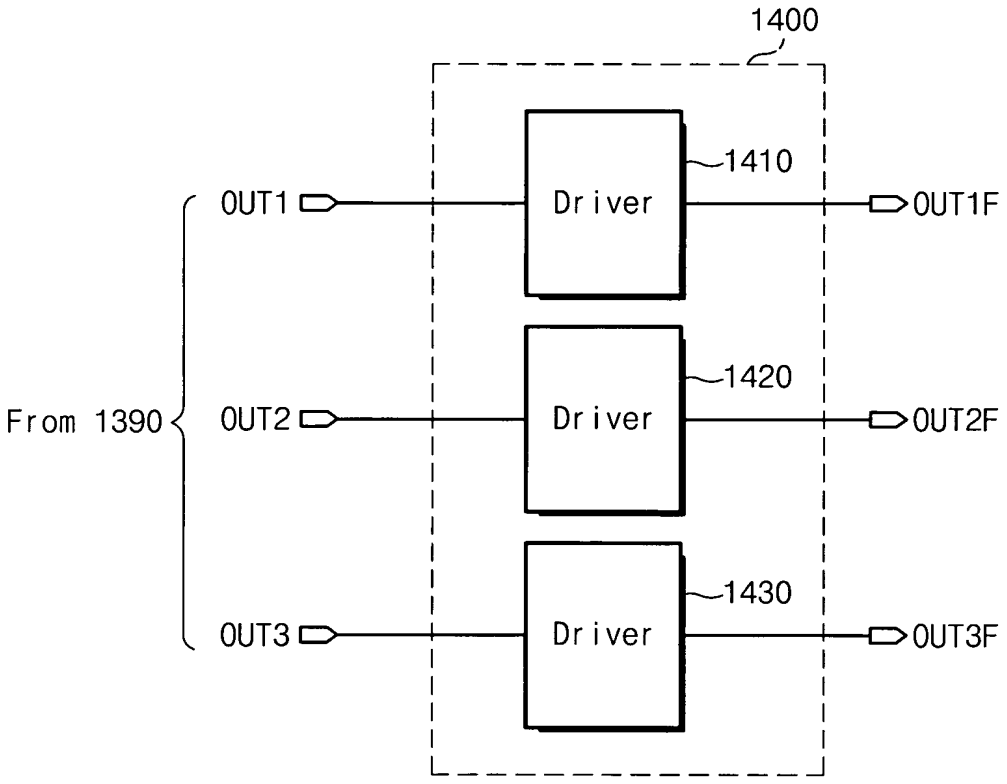

1400
1410
Driver
OUT1
OUT1F
From 1390
1420
Driver
OUT2
OUT2F
1430
Driver
OUT3
OUT3F

Fig. 11

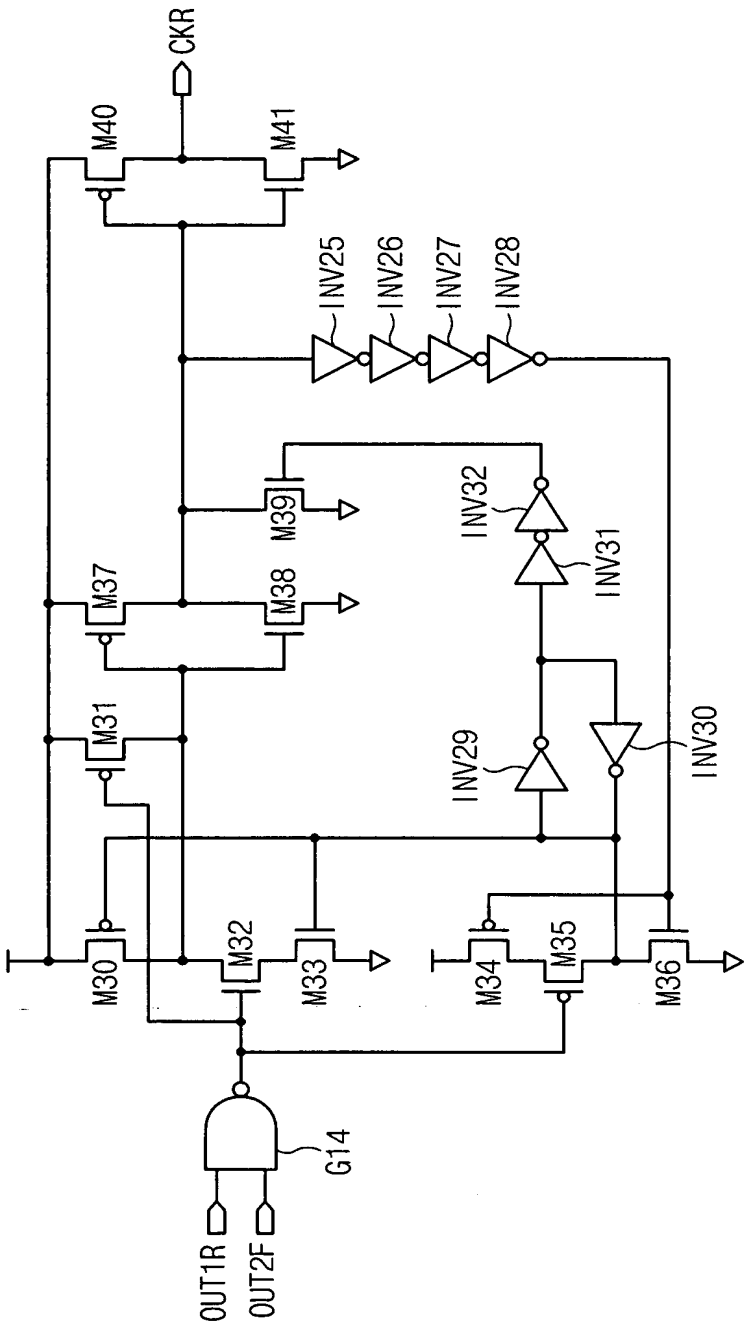
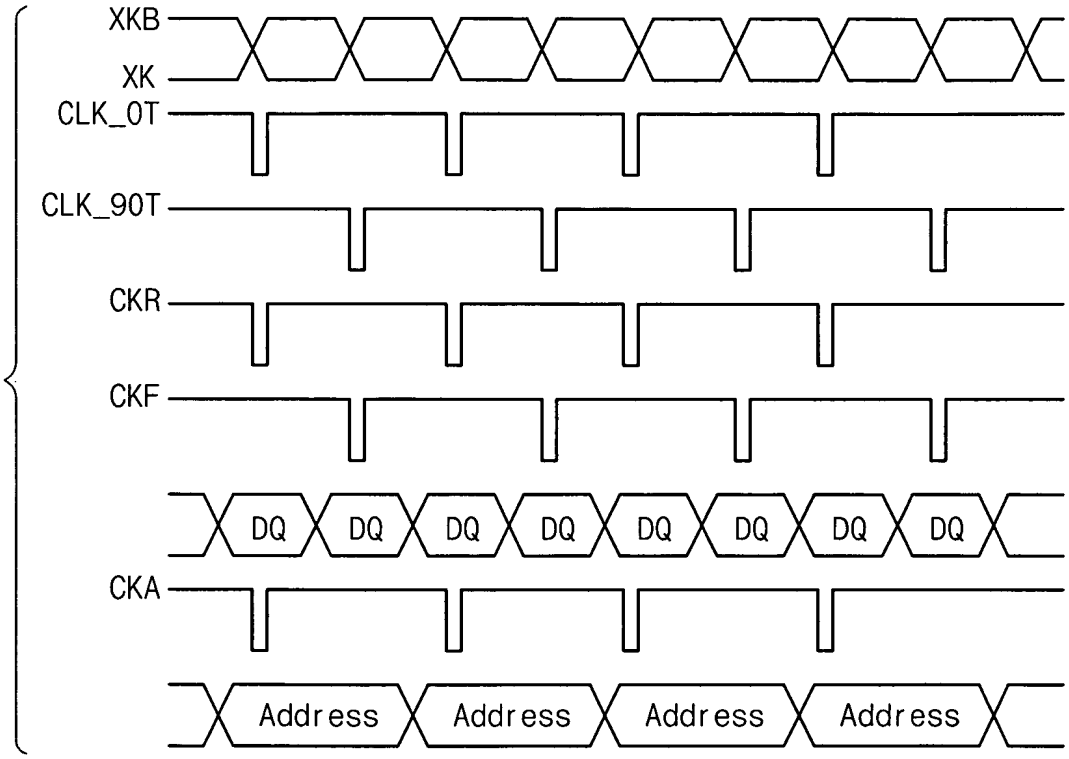
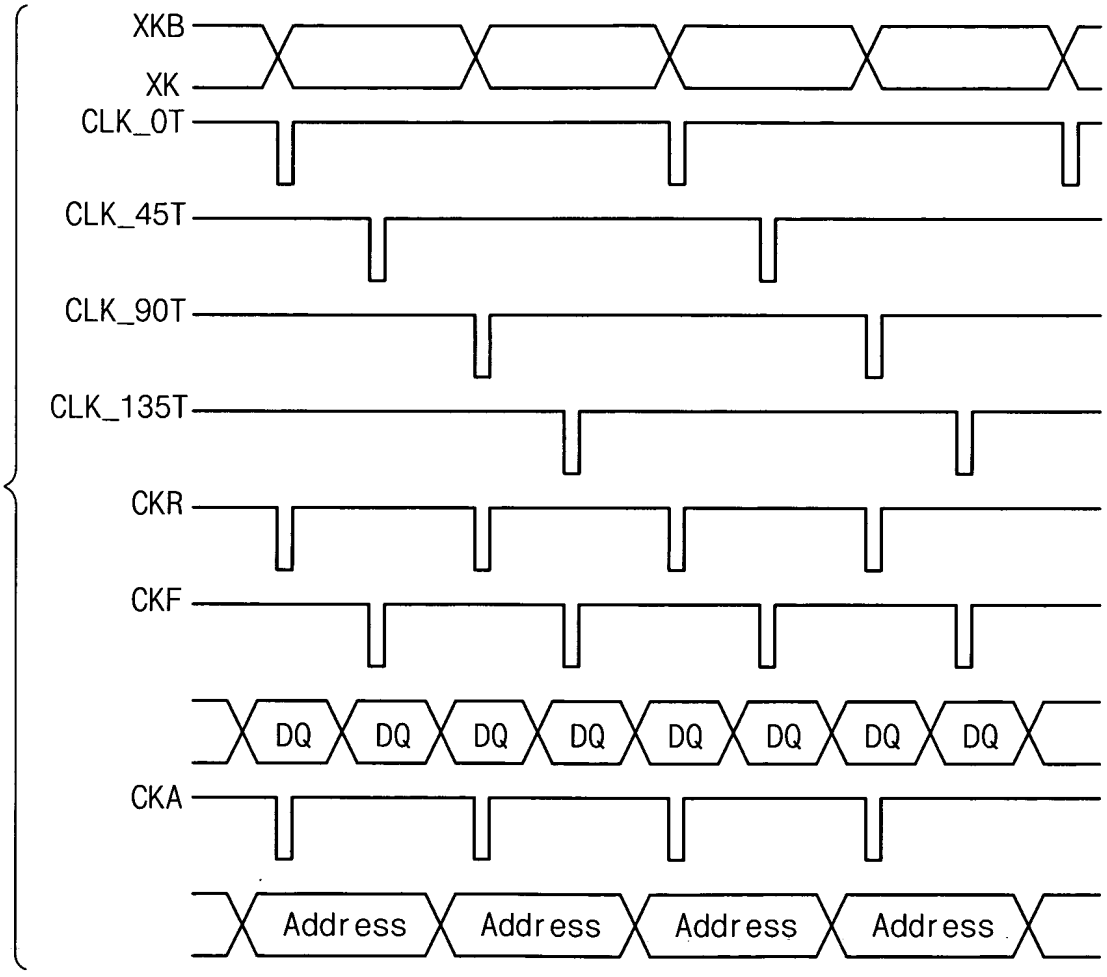

1250
CKR
M40
M41
INV25
INV26
INV27
INV28
M39
INV32
INV31
M37
M38
M31
INV29
INV30
M30
M32
M33
M34
M35
M36
G14
OUT1R
OUT2F

Fig. 12



(Normal Mode)

Fig. 13



(Test Mode)